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	Efferenn et al.	§	Issued: August 28, 2007
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Serial No.:	10/501,464	§	Group Art Unit: 1765
		§	
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For: METHOD FOR MASKING A RECESS IN A STRUCTURE HAVING A HIGH ASPECT RATIO

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July 1, 2008 /Joseph M. Jong/
Date Joseph M. Jong

Dear Sir:

REQUEST FOR A CORRECTED PATENT IN LIEU OF A CERTIFICATE OF CORRECTION

The issued patent for this application erroneously reflects the original translation of the specification and the claims rather than the substitute specification and the amended claims. To show the amendments made to the specification and the claims, attached are the marked-up copy of the substitute specification and the claims section of the preliminary amendment, both filed on July 14, 2004, along with the original application. A clean copy of the substitute specification and a clean copy of the amended claims are also attached for your convenience.

Applicants submit that the errors mentioned above were not by the applicants, but were made during the printing of the patent.

Applicants believe that the nature of the mistake on the part of the Office is such that a certificate of correction is deemed inappropriate in form and respectfully request that the Director issue a corrected patent in lieu thereof as a more appropriate form for certificate of correction, without expense to the patentee.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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SUBSTITUTE SPECIFICATION (MARKED COPY)

~~Description~~

METHOD FOR MASKING A RECESS IN A STRUCTURE HAVING A HIGH ASPECT RATIO

CLAIM FOR PRIORITY

This application is a U.S. national stage of International Application No. PCT/EP03/00087 which was filed in the German language on January 8, 2003, which claims the benefit of priority to Germany application 102 01 178.8 filed January 15, 2002.

TECHNICAL FIELD OF THE INVENTION

The invention relates to a method for masking a recess in a structure, in particular a semiconductor structure, having a high aspect ratio.

BACKGROUND OF THE INVENTION

Masking of recesses is an essential process, in particular in semiconductor technology, and is used to select areas and to process them further independently of areas which are not selected. Normally, photoresists are used for selection of areas and are applied to a semiconductor wafer, the photoresists are then chemically changed in selected areas by means of structured exposure to light, so that the photoresist layer can be removed in the selected areas while it is not removed in the areas which are not selected. The surface of the semiconductor wafer is thus exposed in the selected areas for further processes, for example the application of a layer or ionization of the selected area.

The known method has the disadvantage, however, that it is necessary to adjust an exposure mask in order to expose the

photoresist to light in the selected areas. This is relatively complex, especially when the dimensions are small, for example when producing a dynamic semiconductor memory.

SUMMARY OF THE INVENTION

The ~~object of the~~ invention ~~is to~~ provides a method which is self-adjusting for masking a recess in a structure having a high aspect ratio.

~~The object of the invention is achieved by the features of Claim 1.~~

~~Further advantageous embodiments of the invention are specified in the dependent claims.~~

~~One major advantage~~In one embodiment of the invention, there is ~~that~~a cavity formation, which occurs owing to the high aspect ratio, that is used to selectively choose the recess having the high aspect ratio. The geometric shape of the structure is thus used directly so that there is no need for specific adjustment of the mask. The method according to the invention can therefore be carried out easily.

An isotropic etching method is preferably used as the etching method.

~~A further improvement in the method is achieved by~~In another embodiment of the invention, ~~applying~~ a sacrificial layer is applied to the surface of the structure. The sacrificial layer further increases the aspect ratio of the structure. It is thus even possible to mask structures whose natural aspect ratio does not allow selection. This

extends the field of application of the method according to the invention.

A filling layer is preferably removed to a defined distance from the surface of the structure. This ensures that areas which are located outside the selected area are not adversely affected by a subsequent etching process. The filling layer is therefore not etched away below the level of the structures in the areas which are not selected.

Experiments have shown that the defined distance is preferably greater than twice the maximum thickness of the filling material formed between a cavity and an adjacent structure. This ensures that filling material is removed completely in the selected recess during the subsequent etching process and, furthermore, that there is no adverse effect on the filling material in areas which are not selected.

The invention can be used for a large number of structures. However, one preferred field of application is use for semiconductor structures, in particular for structures which are formed from a silicon material.

A silicon oxide layer is preferably applied as the filling material, and is deposited using a TEOS process. The use of the TEOS process allows cavities to be formed reliably between structures which have more than a specific aspect ratio.

Silicon oxide is preferably deposited as the sacrificial layer. The use of silicon oxide offers the advantage that silicon oxide can be deposited easily and can be removed reliably and selectively after the deposition process.

BRIEF DESCRIPTION OF THE IVENTION

The invention will be explained in more detail in the following text with reference to the figures, in which:

Figure 1 shows ~~a schematic illustration of~~ structures having a high aspect ratio and a low aspect ratio~~,~~.

Figure 2 shows a filled structure with cavities~~,~~.

Figure 3 shows an arrangement for depositing a filling layer~~,~~.

Figure 4 shows a structure with a cavity and a partially removed filling layer~~,~~.

Figure 5 shows a mask for selected areas~~, and~~.

Figure 6 shows a structure with a sacrificial layer.

DETAILED DESCRIPTION OF THE IVENTION

The invention will be explained in the following text with reference to the example of a structure in the form of a silicon material. The method according to the invention may, however, be applied to any type of structure which allows the deposition of the materials used and the application of the processes used. In particular, the method according to the invention can be used for semiconductor materials, such as gallium arsenide.

Figure 1 shows, schematically, a partial detail of a structure which, by way of example, has been produced from a silicon wafer 3. The structure has a first area with webs 4 and first recesses 1, which have a high aspect ratio. The structure furthermore has a second area with webs 4 and a second recess 2, which have a low aspect ratio. The aspect

ratio is defined by the width W with respect to the depth T of the recess. In the illustrated exemplary embodiment, the structure has four webs 4 of equal height, although the distance between a first and a second web 4a, 4b and between the second and a third web 4b, 4c is the same and is less than the distance between the third web 4c and a fourth web 4d.

Instead of the illustrated structure 4, webs of different height and/or webs of different width may also be used. The essential feature in this case is that first recesses 1 with a high aspect ratio and second recesses 2 with a low aspect ratio are formed. The webs 4 are formed from a silicon wafer 3, for example using an etching method. Furthermore, it is also possible for both the webs 4 and a plate from which the webs 4 project to be formed from different materials. For example, the webs 4 may also be formed from a different material on a silicon wafer. By way of example, the webs 4 may be produced from silicon oxide or silicon nitride, or else from a metallic alloy.

Figure 2 shows the silicon wafer 3 after the deposition of a filling layer 5, which is represented in the illustrated exemplary embodiment by a silicon oxide which has been deposited using a TEOS process.

Instead of silicon oxide, any other type of material can be deposited which results in the formation of cavities when a specific aspect ratio is exceeded, and which can be removed again in a subsequent process. The deposition process is defined in such a way that cavities 6 are formed in the first recesses 1, which have a high aspect ratio. In the illustrated exemplary embodiment, a cavity 6 is formed in each first recess 1. However, the deposition process can also be used in such a way that a number of cavities 6 are

formed in a first recess 1. ~~The~~ One important feature in this case is that no cavity is formed in the second recess 2, which has a lower aspect ratio. The formation of cavities 6 depends on the aspect ratio of the filled structure. The filling material used and the deposition process used can be matched to the existing aspect ratios of the structure such that cavities 6 are produced in desired recesses 1.

The TEOS process which is used offers the advantage that the edge structure of the present structure, on which the TEOS material is deposited, likewise, to a certain extent, models the edge structure. In this way, cavities 6 are formed in structures having a high aspect ratio which is greater than a defined value. The defined value depends on the deposition process that is used.

Figure 3 shows ~~a schematic illustration of~~ an apparatus for depositing a layer using a TEOS process. An organic liquid is used as the silicon source during the deposition process. The oxide which is produced from the vapour of the liquid is highly electrically stable in addition to providing conformal step coverage. During the deposition process, silicon oxide is deposited in accordance with the following formula:

$$SiO_4C_8H_{20} \rightarrow 725°C \rightarrow SiO_2 \ ...$$

Other liquid sources for silicon oxide deposition are diethylsilane, ditertiary butylsilane and tetramethyl-cyclotetrasiloxane. These liquid sources allow the deposition temperature to be reduced to 380 to 650°C. Figure 3 shows, schematically, a quartz tube in which a large number of silicon wafers 3 are arranged. The quartz tube is connected via a line to a gas area which is formed

above a liquid gas source 7. The liquid gas source 7 is kept at a defined temperature by a heat source 8. Furthermore, both the liquid gas and the quartz tube are supplied with nitrogen oxide. In addition, the quartz tube is connected to a vacuum pumping system 10 via a vacuum valve 9. The vacuum pumping system ensures that there is a defined pressure in the quartz tube. The quartz tube is surrounded by a three-zone oven 11, which also ensures that there is a defined temperature in the quartz tube. The deposition of TEOS silicon is a known method, so that the details will not be described here. The TEOS process is, for example, described in Section 7.1.2.2 "Low Pressure CVD-Verfahren" [Low pressure CVD processes] of "Siliziumhalbleitertechnologie" [Silicon semiconductor technology] Hilleringmann, Teubner, 1999, ISBN 3-519-10149-1. A major feature of the deposition process that is used is that the cavities 6 extend as far as an area which is located above the upper edge of the webs 4.

In a further method step, the filling layer 5 ~~must be~~ is removed in a planar manner as far as the area of the cavities 6. The filling layer 5 is preferably removed until the cavities 6 are opened. However, depending on the application, it may be advantageous to allow a certain residual thickness to remain above the cavities 6.

When using a planar removal process, the filling layer 5 is removed, for example, by means of a chemical, mechanical polishing method. The filling layer 5 is preferably removed to a distance α with respect to the upper edge of the webs 4. The distance α is preferably chosen such that α is greater than or equal to twice the maximum distance β between a cavity boundary and the surrounding structure. Figure 3 shows the distance β between one surface of a cavity 6 and a corner area between a web 4 and the plate of

the silicon wafer 3. The choice of the defined distance ensures that the filling material 5 is completely removed from the first recesses 1 during the subsequent etching process without etching underneath the webs 4, which bound the second recess 2, at the sides.

The filling layer 5 is then etched away in a subsequent method step, by means of an etching method, preferably an anisotropic etching method. In the process, the etching solution which is used, such as alkali lyes or dry etching methods such as plasma etching, attacks in the area of the cavity 6 and etches the filling layer 5 out of the first recesses 1. At the same time, the etching solution also attacks the upper face of the filling layer 5 in the area of the second recess 2. However, only the surface of the filling layer 5 is etched away owing to the distance which is chosen. The distance α was chosen such that no etching underneath the webs occurs in the area of the second recesses 2. The etching process is stopped when the filling layer 5 has been removed from the first recess 1.

After the removal of the filling layer 5 from the first recesses 1, an arrangement is obtained as is illustrated in Figure 5.

The method according to the invention results in the surfaces which are arranged in the first recesses 1 being exposed. Surfaces of other recesses, such as the second recess 2, are still covered by the filling layer 5. The filling layer 5 thus forms a covering mask for areas of the semiconductor wafer 3 which are not selected.

The exposed areas, in this case the first recesses 1, can be used in the rest of the method for, for example, implantation, for further etching, or for selective growth

of a material such as silicon, silicon oxide or silicon nitride.

Owing to the method according to the invention, there is no need to use an adjustment process for an etching mask. The mask is adjusted on the basis of the use of the geometry of the structure and cavity formation during the deposition process that is used, without any adjustment being required.

Figure 6 shows a further development of the method according to the invention, in which a sacrificial layer 12 is applied in a defined thickness γ on the webs 4. The sacrificial layer 12 may, for example, be in the form of silicon oxide or silicon nitride. The structure is not filled with the filling layer 5 until the sacrificial layer 12 has been applied. The sacrificial layer 12 offers the advantage that the height of the webs 4 is increased, so that the aspect ratio becomes higher. The aspect ratio can thus be set in such a way that the cavities 6 are formed in the desired way in the first recesses 1. The further processes such as removal of the filling layer 5 are carried out in accordance with the method described above.

Figure 6 shows the structure with a sacrificial layer 12, in which the filling layer 5 has already been removed once again as far as the cavities 6. The formation of the sacrificial layer 12 preferably makes it possible to remove the filling layer 5 as far as the upper side of the sacrificial layer 12. It is thus simple to control the removal process, since the depth of the filling layer 5 which is removed is governed by the height of the sacrificial layer 12. In this embodiment as well, it is advantageous for there to be a distance between the upper edge of the sacrificial layer 12 and an upper edge of the

removed sacrificial layer 12, as is shown in Figure 6. The distance α can be selected in this way: $\alpha \geq 2\beta - \gamma$, where β denotes the maximum distance between a cavity boundary of a cavity 6 and the structure of the silicon wafer 3 or of a web 4, and γ denotes the height of the sacrificial layer 12. At the end of the process, the sacrificial layer 12 is removed once again, for example using a selective etching method.

List of reference symbols

1	1st recess
2	2nd recess
3	Silicon wafer
4	Web
5	Filling layer
6	Cavities
7	Liquid gas source
8	Heat source
9	Valve
10	Vacuum pumping system
11	Three-zone oven
12	Sacrificial layer

AMENDMENTS TO THE CLAIMS

Please replace the claims, including all prior versions, with the listing of claims below.

Listing of Claims:

1. (Currently amended) ~~Method~~A method for masking first recesses ~~(1)~~ in a structure ~~(4)~~ having webs ~~(4)~~ with a high aspect ratio, comprising a set of recesses ~~(1, 2)~~ having different aspect ratios, ~~in particular a semiconductor structure, having the following steps~~comprising:

- applying a filling layer ~~(5) is applied~~ to the structure ~~(1, 2, 4)~~,

with the filling layer ~~(5) being~~ applied over a fixed distance beyond the webs ~~(4) in~~ such ~~a way~~ that a cavity ~~(6)~~ is formed in the first recesses ~~(1)~~ having a high aspect ratio~~;~~;

- removing the filling layer ~~(5) is removed~~ by means of a planar removal process into ~~the~~an area of the cavity ~~(6)~~ with the filling layer ~~(5) being~~ removed to a defined distance above ~~the~~a surface of the webs ~~(4)~~;

- removing the filling layer ~~(5) is removed~~ in an etching process, with the etching process ~~also~~ attacking in the cavity ~~(6)~~ and, owing to the cavity ~~(6)~~, the filling layer ~~(5) being~~ removed more quickly from the first recess ~~(1)~~ than from recesses ~~(2)~~ without a cavity ~~(6)~~, and ~~with~~ the etching process being stopped after removal of the filling layer ~~(5)~~ from the first recess ~~(1)~~, with the defined distance being ~~chosen~~ selected such that the webs ~~(4)~~ are not underetched in ~~the~~an area of a recess ~~(2)~~ with a low aspect ratio during the etching process.

2. (Currently amended) ~~Method~~ The method according to Claim 1, ~~characterized in that~~wherein an isotropic etching method is used as the etching method.

3. (Currently amended) ~~Method~~ The method according to ~~one of Claims 1 or 2, characterized in that~~claim 1, wherein the structure ~~(1, 2, 4)~~ has the webs ~~(4)~~, and ~~in that~~ a sacrificial layer ~~(12)~~ is applied to the surface of the webs ~~(4),~~ before the application of the filling layer ~~(5)~~.

4. (Currently amended) ~~Method~~ The method according to ~~one of Claims 1 to 3, characterized in that~~claim 1, wherein a chemical/mechanical polishing method is used as ~~the~~ a planar removal process.

5. (Currently amended) ~~Method~~ The method according to Claim 4, ~~characterized in that~~wherein the defined distance is chosen to be greater than twice ~~the~~ a maximum thickness ~~(β)~~ of the filling material ~~(5)~~ between ~~a~~the cavity ~~(6)~~ and the structure ~~(4, 3)~~.

6. (Currently amended) ~~Method~~ The method according to ~~one of Claims 1 to 5, characterized in that~~claim 1, wherein the structure ~~(1, 2, 4)~~ is formed from a silicon wafer ~~(3)~~.

7. (Currently amended) ~~Method~~ The method according to ~~one of Claims 1 to 6, characterized in that~~claim 1, wherein a silicon oxide is deposited as the filling layer ~~(5)~~, using a TEOS process.

8. (Currently amended) ~~Method~~ The method according to ~~one of Claims 1 to 7, characterized in that~~claim 1, wherein silicon oxide is deposited as the sacrificial layer ~~(12)~~.

9. (Currently amended) ~~Method~~ The method according to ~~one of Claims 1 to 8, characterized in that~~claim 1, wherein the filling layer ~~(5)~~ is applied over a recess ~~(2)~~ with a low aspect ratio to above ~~the~~a height of the cavity ~~(6)~~.

METHOD FOR MASKING A RECESS IN A STRUCTURE HAVING A HIGH ASPECT RATIO

CLAIM FOR PRIORITY

This application is a U.S. national stage of International Application No. PCT/EP03/00087 which was filed in the German language on January 8, 2003, which claims the benefit of priority to Germany application 102 01 178.8 filed January 15, 2002.

TECHNICAL FIELD OF THE INVENTION

The invention relates to a method for masking a recess in a structure, in particular a semiconductor structure, having a high aspect ratio.

BACKGROUND OF THE INVENTION

Masking of recesses is an essential process, in particular in semiconductor technology, and is used to select areas and to process them further independently of areas which are not selected. Normally, photoresists are used for selection of areas and are applied to a semiconductor wafer, the photoresists are then chemically changed in selected areas by means of structured exposure to light, so that the photoresist layer can be removed in the selected areas while it is not removed in the areas which are not selected. The surface of the semiconductor wafer is thus exposed in the selected areas for further processes, for example the application of a layer or ionization of the selected area.

The known method has the disadvantage, however, that it is necessary to adjust an exposure mask in order to expose the photoresist to light in the selected areas. This is

relatively complex, especially when the dimensions are small, for example when producing a dynamic semiconductor memory.

SUMMARY OF THE INVENTION

The invention provides a method which is self-adjusting for masking a recess in a structure having a high aspect ratio.

In one embodiment of the invention, there is a cavity formation, which occurs owing to the high aspect ratio, that is used to selectively choose the recess having the high aspect ratio. The geometric shape of the structure is thus used directly so that there is no need for specific adjustment of the mask. The method according to the invention can therefore be carried out easily.

An isotropic etching method is preferably used as the etching method.

In another embodiment of the invention, a sacrificial layer is applied to the surface of the structure. The sacrificial layer further increases the aspect ratio of the structure. It is thus even possible to mask structures whose natural aspect ratio does not allow selection. This extends the field of application of the method according to the invention.

A filling layer is preferably removed to a defined distance from the surface of the structure. This ensures that areas which are located outside the selected area are not adversely affected by a subsequent etching process. The filling layer is therefore not etched away below the level of the structures in the areas which are not selected.

Experiments have shown that the defined distance is preferably greater than twice the maximum thickness of the filling material formed between a cavity and an adjacent structure. This ensures that filling material is removed completely in the selected recess during the subsequent etching process and, furthermore, that there is no adverse effect on the filling material in areas which are not selected.

The invention can be used for a large number of structures. However, one preferred field of application is use for semiconductor structures, in particular for structures which are formed from a silicon material.

A silicon oxide layer is preferably applied as the filling material, and is deposited using a TEOS process. The use of the TEOS process allows cavities to be formed reliably between structures which have more than a specific aspect ratio.

Silicon oxide is preferably deposited as the sacrificial layer. The use of silicon oxide offers the advantage that silicon oxide can be deposited easily and can be removed reliably and selectively after the deposition process.

BRIEF DESCRIPTION OF THE IVENTION

The invention will be explained in more detail in the following text with reference to the figures, in which:

Figure 1 shows structures having a high aspect ratio and a low aspect ratio.

Figure 2 shows a filled structure with cavities.

Figure 3 shows an arrangement for depositing a filling layer.

Figure 4 shows a structure with a cavity and a partially removed filling layer.

Figure 5 shows a mask for selected areas.

Figure 6 shows a structure with a sacrificial layer.

DETAILED DESCRIPTION OF THE IVENTION

The invention will be explained in the following text with reference to the example of a structure in the form of a silicon material. The method according to the invention may, however, be applied to any type of structure which allows the deposition of the materials used and the application of the processes used. In particular, the method according to the invention can be used for semiconductor materials, such as gallium arsenide.

Figure 1 shows, schematically, a partial detail of a structure which, by way of example, has been produced from a silicon wafer 3. The structure has a first area with webs 4 and first recesses 1, which have a high aspect ratio. The structure furthermore has a second area with webs 4 and a second recess 2, which have a low aspect ratio. The aspect ratio is defined by the width W with respect to the depth T of the recess. In the illustrated exemplary embodiment, the structure has four webs 4 of equal height, although the distance between a first and a second web 4a, 4b and between the second and a third web 4b, 4c is the same and is less than the distance between the third web 4c and a fourth web 4d.

Instead of the illustrated structure 4, webs of different height and/or webs of different width may also be used. The essential feature in this case is that first recesses 1 with a high aspect ratio and second recesses 2 with a low aspect ratio are formed. The webs 4 are formed from a silicon wafer 3, for example using an etching method. Furthermore, it is also possible for both the webs 4 and a plate from which the webs 4 project to be formed from different materials. For example, the webs 4 may also be formed from a different material on a silicon wafer. By way of example, the webs 4 may be produced from silicon oxide or silicon nitride, or else from a metallic alloy.

Figure 2 shows the silicon wafer 3 after the deposition of a filling layer 5, which is represented in the illustrated exemplary embodiment by a silicon oxide which has been deposited using a TEOS process.

Instead of silicon oxide, any other type of material can be deposited which results in the formation of cavities when a specific aspect ratio is exceeded, and which can be removed again in a subsequent process. The deposition process is defined in such a way that cavities 6 are formed in the first recesses 1, which have a high aspect ratio. In the illustrated exemplary embodiment, a cavity 6 is formed in each first recess 1. However, the deposition process can also be used in such a way that a number of cavities 6 are formed in a first recess 1. One important feature in this case is that no cavity is formed in the second recess 2, which has a lower aspect ratio. The formation of cavities 6 depends on the aspect ratio of the filled structure. The filling material used and the deposition process used can be matched to the existing aspect ratios of the structure such that cavities 6 are produced in desired recesses 1.

The TEOS process which is used offers the advantage that the edge structure of the present structure, on which the TEOS material is deposited, likewise, to a certain extent, models the edge structure. In this way, cavities 6 are formed in structures having a high aspect ratio which is greater than a defined value. The defined value depends on the deposition process that is used.

Figure 3 shows an apparatus for depositing a layer using a TEOS process. An organic liquid is used as the silicon source during the deposition process. The oxide which is produced from the vapour of the liquid is highly electrically stable in addition to providing conformal step coverage. During the deposition process, silicon oxide is deposited in accordance with the following formula:

$$SiO_4C_8H_{20} \rightarrow 725°C \rightarrow SiO_2 \ldots$$

Other liquid sources for silicon oxide deposition are diethylsilane, ditertiary butylsilane and tetramethyl-cyclotetrasiloxane. These liquid sources allow the deposition temperature to be reduced to 380 to 650°C. Figure 3 shows, schematically, a quartz tube in which a large number of silicon wafers 3 are arranged. The quartz tube is connected via a line to a gas area which is formed above a liquid gas source 7. The liquid gas source 7 is kept at a defined temperature by a heat source 8. Furthermore, both the liquid gas and the quartz tube are supplied with nitrogen oxide. In addition, the quartz tube is connected to a vacuum pumping system 10 via a vacuum valve 9. The vacuum pumping system ensures that there is a defined pressure in the quartz tube. The quartz tube is surrounded by a three-zone oven 11, which also ensures that there is a defined temperature in the quartz tube. The deposition of TEOS silicon is a known method, so that the

details will not be described here. The TEOS process is, for example, described in Section 7.1.2.2 "Low Pressure CVD-Verfahren" [Low pressure CVD processes] of "Siliziumhalbleitertechnologie" [Silicon semiconductor technology] Hilleringmann, Teubner, 1999, ISBN 3-519-10149-1. A major feature of the deposition process that is used is that the cavities 6 extend as far as an area which is located above the upper edge of the webs 4.

In a further method step, the filling layer 5 is removed in a planar manner as far as the area of the cavities 6. The filling layer 5 is preferably removed until the cavities 6 are opened. However, depending on the application, it may be advantageous to allow a certain residual thickness to remain above the cavities 6.

When using a planar removal process, the filling layer 5 is removed, for example, by means of a chemical, mechanical polishing method. The filling layer 5 is preferably removed to a distance α with respect to the upper edge of the webs 4. The distance α is preferably chosen such that α is greater than or equal to twice the maximum distance β between a cavity boundary and the surrounding structure. Figure 3 shows the distance β between one surface of a cavity 6 and a corner area between a web 4 and the plate of the silicon wafer 3. The choice of the defined distance ensures that the filling material 5 is completely removed from the first recesses 1 during the subsequent etching process without etching underneath the webs 4, which bound the second recess 2, at the sides.

The filling layer 5 is then etched away in a subsequent method step, by means of an etching method, preferably an anisotropic etching method. In the process, the etching solution which is used, such as alkali lyes or dry etching

methods such as plasma etching, attacks in the area of the cavity 6 and etches the filling layer 5 out of the first recesses 1. At the same time, the etching solution also attacks the upper face of the filling layer 5 in the area of the second recess 2. However, only the surface of the filling layer 5 is etched away owing to the distance which is chosen. The distance α was chosen such that no etching underneath the webs occurs in the area of the second recesses 2. The etching process is stopped when the filling layer 5 has been removed from the first recess 1.

After the removal of the filling layer 5 from the first recesses 1, an arrangement is obtained as is illustrated in Figure 5.

The method according to the invention results in the surfaces which are arranged in the first recesses 1 being exposed. Surfaces of other recesses, such as the second recess 2, are still covered by the filling layer 5. The filling layer 5 thus forms a covering mask for areas of the semiconductor wafer 3 which are not selected.

The exposed areas, in this case the first recesses 1, can be used in the rest of the method for, for example, implantation, for further etching, or for selective growth of a material such as silicon, silicon oxide or silicon nitride.

Owing to the method according to the invention, there is no need to use an adjustment process for an etching mask. The mask is adjusted on the basis of the use of the geometry of the structure and cavity formation during the deposition process that is used, without any adjustment being required.

Figure 6 shows a further development of the method according to the invention, in which a sacrificial layer 12 is applied in a defined thickness γ on the webs 4. The sacrificial layer 12 may, for example, be in the form of silicon oxide or silicon nitride. The structure is not filled with the filling layer 5 until the sacrificial layer 12 has been applied. The sacrificial layer 12 offers the advantage that the height of the webs 4 is increased, so that the aspect ratio becomes higher. The aspect ratio can thus be set in such a way that the cavities 6 are formed in the desired way in the first recesses 1. The further processes such as removal of the filling layer 5 are carried out in accordance with the method described above.

Figure 6 shows the structure with a sacrificial layer 12, in which the filling layer 5 has already been removed once again as far as the cavities 6. The formation of the sacrificial layer 12 preferably makes it possible to remove the filling layer 5 as far as the upper side of the sacrificial layer 12. It is thus simple to control the removal process, since the depth of the filling layer 5 which is removed is governed by the height of the sacrificial layer 12. In this embodiment as well, it is advantageous for there to be a distance between the upper edge of the sacrificial layer 12 and an upper edge of the removed sacrificial layer 12, as is shown in Figure 6. The distance α can be selected in this way: $\alpha \geq 2\beta - \gamma$, where β denotes the maximum distance between a cavity boundary of a cavity 6 and the structure of the silicon wafer 3 or of a web 4, and γ denotes the height of the sacrificial layer 12. At the end of the process, the sacrificial layer 12 is removed once again, for example using a selective etching method.

List of reference symbols

1	1st recess
2	2nd recess
3	Silicon wafer
4	Web
5	Filling layer
6	Cavities
7	Liquid gas source
8	Heat source
9	Valve
10	Vacuum pumping system
11	Three-zone oven
12	Sacrificial layer

CLEAN COPY OF AMENDED CLAIMS

1. A method for masking first recesses in a structure having webs with a high aspect ratio, comprising a set of recesses having different aspect ratios, comprising:

applying a filling layer to the structure, with the filling layer applied over a fixed distance beyond the webs such that a cavity is formed in the first recesses having a high aspect ratio;

removing the filling layer by means of a planar removal process into an area of the cavity with the filling layer removed to a defined distance above a surface of the webs;

removing the filling layer in an etching process, with the etching process attacking in the cavity and, owing to the cavity, the filling layer removed more quickly from the first recess than from recesses without a cavity, and the etching process being stopped after removal of the filling layer from the first recess, with the defined distance being selected such that the webs are not underetched in an area of a recess with a low aspect ratio during the etching process.

2. The method according to Claim 1, wherein an isotropic etching method is used as the etching method.

3. The method according to claim 1, wherein the structure has the webs, and a sacrificial layer is applied to the surface of the webs before the application of the filling layer.

4. The method according to claim 1, wherein a chemical/mechanical polishing method is used as a planar removal process.

5. The method according to Claim 4, wherein the defined distance is chosen to be greater than twice a maximum thickness of the filling material between the cavity and the structure.

6. The method according to claim 1, wherein the structure is formed from a silicon wafer.

7. The method according to claim 1, wherein a silicon oxide is deposited as the filling layer, using a TEOS process.

8. The method according to claim 1, wherein silicon oxide is deposited as the sacrificial layer.

9. The method according to claim 1, wherein the filling layer is applied over a recess with a low aspect ratio to above a height of the cavity.